REMARKS

The Advisory Action mailed on November 21, 2008, has been received and its contents carefully considered. It is respectfully submitted that the final rejections be reconsidered, and an RCE is filed herewith under 37 CFR §1.114, together with a Petition for One Month's Extension of Time, thereby extending the period for reply to December 5, 2008.

As the Amendment filed November 5, 2008 has **not** been entered, this Amendment includes the same changes as well as additional changes to the claims.

In this Amendment, Applicants have amended claim 1 and added new claims 8-11. Claim 1 is the only independent claim pending and under consideration, and claims 1-4 and 8-11 are pending and under consideration in the application, claims 5-7 having been withdrawn from consideration. For at least the following reasons, it is submitted that this application is in condition for allowance.

Newly added claims 8 and 10 are supported by ¶[0034] of the specification as originally filed:

> [0034] In the example shown in FIG. 1, the upper electrode **8** is formed, as a p-side electrode because the p-type layer **5** exists on a top side of the semiconductor lamination portion **6**, with a lamination structure made of, for example, Ti/Au, Pd/Au, Ni/Au or the like and having a thickness of approximately 0.2 to 1 μm in total. The lower electrode (an n-side electrode) **9** is formed with an alloy layer made of, for example, Ti-Al, Ti-Au or the like, and having a thickness of approximately 0.2 to 1 μm in total.

Newly added claim 9 is supported by ¶[0030] of the specification as originally filed:

> [0030] Although an example in which the n-type layer **3** and the p-type layer **5** are formed with a single layer is shown in the example shown in FIG. 1, generally, for example, they are formed with a structure where a GaN layer with which it is easy to enhance a carrier density is formed as a contact layer at an electrode forming portion, and where, occasionally, an AlGaN based compound which has a larger band gap energy than that of the active layer is employed in order to confine carriers easily at a side of the active layer, and furthermore they can be formed with a multi-layer structure to give other functions. And a structure with a superlattice can be applied in order to laminate layers of different lattice constants. But a single layer which has the above described functions can be employed. And although a thickness of each layer is set depending upon objects respectively, for example, the n-type layer **3** is formed having a thickness of approximately 3 to 10 μm in total, and the p-type layer **5** is formed having a thickness of approximately 0.1 to 1 μm in total. In addition, the n-type layer **3** is formed by doping gallium nitride based compound semiconductor with dopants such as Se, Si, Ge, Te or the like and the p-type layer **5** is formed by doping the same with dopants such as Mg, Zn or the like.

Newly added claim 11 is supported by ¶[0033] of the specification as originally filed:

> [0033] The light transmitting conductive layer **7** is formed having a thickness of approximately 2 to 100 nm by alloying Ni and Au previously laminated or with a ZnO layer, an ITO layer or the like which is light transmitting, conductive to disperse the electric current to whole surface of a chip, and easy to get an ohmic contact with the p-type layer **5**. The ZnO layer or the ITO layer is formed having a thickness of approximately 0.3 to 2 μm, because they transmit light even if thick. In the example shown in FIG. 1, the ZnO layer having a thickness of approximately 0.3 μm is formed as the light transmitting conductive layer **7**.

In the present invention an electric current blocking portion is formed on an exposed surface of the p-type layer of the semiconductor lamination portion exposed by removing a part of the light transmitting conductive layer for preventing current from flowing into the lower side of the upper electrode as much as possible since light emitted upon flow of current to the lower side of the upper electrode cannot be effectively extracted, and in that the upper electrode is formed on the electric current blocking portion, so as to adhere to the semiconductor lamination portion and to be in contact with the light transmitting conductive layer on a periphery of the part removed.

Claim 1 presently recites "an upper electrode formed so as to be in contact with an exposed surface of the p-type layer of the semiconductor lamination portion exposed by removing a part of the light transmitting conductive layer, and to be in contact with the light transmitting conductive layer on a periphery of the part removed; and *an electric current blocking portion formed on the exposed surface of the semiconductor lamination portion*, the electric current blocking portion preventing electric current from flowing into a part of the semiconductor lamination portion under the upper electrode through the electric current blocking portion".

In the Response to Arguments, the Examiner alleges that an "electric current blocking section" is taught by removed portions of light transmitting conductive layers **60** in *Kunisato et al.* (US 5,990,496) and **44** in *Chang et al.* (US

6,583,443 B1) respectively. The *Kunisato et al.* and *Chang et al.* references will be discussed with respect to each rejection as appropriate.

Claims 1-2 and 4 were rejected under 35 USC §102(b) as anticipated by, or alternatively under 35 USC §103(a) as obvious solely over, *Kunisato et al.* (US 5,990,496). These rejections are each respectfully traversed.

The Office Action asserts that the layer **60** of *Kunisato et al.* is a light transmitting conductive layer. However, this layer **60** is a *current blocking layer* of SiO_2, SiN, or n-type GaN, as described in column 11, lines 6 to 10 thereof:

> An SiO_2, SiN, or n-type GaN current blocking layer **60** having a stripe-like opening in the center is formed on the p-type GaN contact layer **59**. A p electrode **61** is formed on the p-type GaN contact layer **59** and an n electrode **62** is formed on the n-type GaN contact layer **54**.

$Si0_2$ or SiN is an insulating layer and cannot be a conductive layer. By being disposed on a p-type GaN contact layer **59**, the n-type GaN layer blocks electric current by forming a pn-junction of reversed direction with the p-electrode **9**. To sum up, this layer is a layer that blocks the electric current from the p-electrode 9 to the p-type GaN contact layer **59** side, so that it is completely different from the *light transmitting conductive layer* of the present invention, which transmits the emitted light while diffusing the electric current from the p-side electrode **8** to the whole surface of the chip of the semiconductor laminate portion **6**.

This is because the device of *Kunisato et al.* is not an LED that emits light from the whole surface of the chip but is a laser diode that emits light from only a part of the region having a stripe shape, and does not radiate light from the surface of the chip but radiates light from the end surface (side surface) of the chip, hence having a completely different function.

Consequently, *Kunisato et al.* fails to teach or suggest "an upper electrode formed so as to be in contact with an exposed surface of the p-type layer of the semiconductor lamination portion exposed by removing a part of the light transmitting conductive layer, and to be in contact with the light transmitting conductive layer on a periphery of the part removed; and *an electric current blocking portion formed on the exposed surface of the semiconductor lamination portion*, the electric current blocking portion preventing electric current from flowing into a part of the semiconductor lamination portion under the upper electrode through the electric current blocking portion" as recited in claim 1.

Accordingly, claim 1 patentably defines over *Kunisato et al.* and is allowable, together with claims 2 and 4 that depend therefrom.

Claims 1-4 were rejected under 35 USC §103(a) as obvious over the combination of *Chang et al.* (US 6,583,443 B1) with *Shakuda et al.* (US 6,107,644). This rejection is respectfully traversed.

Chang et al. discloses an LED in which a transparent conductive layer **44** (n-type ohmic contact transparent electrode **35** of FIG. 3C, 3D and 3E) is formed

on the etch stop layer **24** of the LED, and a metal layer **48B** is formed on a surface of the etch stop layer **24** that is exposed by removing a part of the transparent conductive layer **44**. However, this etch stop layer **24** is preferably InGaP or AlGaAs, and there is no disclosure of a gallium nitride based compound as in the present invention, so that it will not be a current blocking region even if it is exposed by removing a part of the transparent electrode. See column 4, lines 23 to 35:

> The preferred material of the etching stop layer **24** according to the present invention can be any III–V compound semiconductor material that has an etching selectively to that of the GaAs substrate **26**. As to the lattice matched with that of the GaAs substrate **26** is not crucial. It's for sure, if the lattice matched well is also preferred because it can reduce the dislocation density. The good candidates of those satisfied above conditions, for examples, InGaP or AlGaAs can be served as the etch stop layer **24**. The lower cladding layer **22** can also be served as the etching stop layer **24** since it has a high selectivity to GaAs substrate **26**, and thus if the thickness of the lower cladding layer **22** is thick enough, the etch stop layer **24** becomes optional.

According to the present invention, an electric current blocking function is exhibited by a surface exposed by performing dry etching on the surface of a gallium nitride based compound.

Moreover, according to *Chang et al.*, the surface side is an n-type layer, and the etch stop layer **24** is also an n-type layer. This is clear from the fact that the GaAs substrate **26** and the lower cladding layer **22** are n-type layers. See column 3, lines 47 to 59:

Referring to FIG. 1, the cross-sectional view shows an epi-LED stack structure comprises, from a bottom thereof, an n-type temporary GaAs substrate **26**, an etching stop layer **24**, a lower cladding layer **22**, an active layer **20** an upper cladding layer **18**, a p-type ohmic contact epi-layer **16** and a p-type metal electrode **28**. The shape of the metal electrode **28** is arbitrary, shown in the figure is a ring shape, so two electrode blocks **28** are observed in a cross-sectional view.

The lower cladding layer **22** is an n-type $(Al_xGa_{1-x})_{0.5}In_{0.5}P$. The active layer **20** is an undoped $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ layer and the upper cladding layer **18** is a p-type $(Al_{x\ or\ 1-x})_{0.5}In_{0.5}P$ layer.

Further, the contact characteristics of the metal layer **48B** with the n-type ohmic contact transparent electrode **35** (see column 5, lines 25 to 26: "Then, an n-type ohmic contact transparent electrode **35** is deposited on the etch stop layer **24** and on the third photoresist resist pattern **34**") and the etch stop layer **24** will have a similar tendency (when viewed from the metal layer **48B**, both are in contact with the n-type transparent conductive layer **44** and the semiconductor layer **24**).

However, according to a preferred embodiment of the present invention, the light transmitting conductive layer is made of an alloy of Au-Ni composition or a material generally exhibiting an n-type such as ZnO or ITO, and the surface of the semiconductor layer **5** that is brought into contact with the upper electrode **8** is a p-type, and the contact characteristics with the upper electrode are different from those of the transmitting conductive layer with the upper electrode, so that it can improve the ohmic contact characteristics between the upper electrode and

the light transmitting conductive layer and can reduce the contact characteristics between the upper electrode and the exposed p-type semiconductor layer.

To sum up, contrasting the present invention and *Chang et al.*, the semiconductor layer that is brought into contact with the upper electrode is made of a different material and has a different electric conductivity even though having the same structure of providing a light transmitting conductive layer on the semiconductor layer, so that the two cannot have the same contact characteristics.

The Office Action alleges that, since *Shakuda et al.* discloses a semiconductor laminate portion made of a gallium nitride based compound semiconductor, it can be used to replace the semiconductor layers of *Chang et al.* However, the present invention uses the current blocking characteristics of the surface exposed by etching the surface of the gallium nitride based compound semiconductor layer. Therefore, as the LED of Chang does not exhibit such current blocking characteristics, there is no reason to apply to the LED of *Chang et al.* the semiconductor laminate portion made of a gallium nitride based compound semiconductor of *Shakuda et al.* that neither teaches nor suggests achieving the current blocking characteristics by etching the gallium nitride based compound semiconductor surface. The reason given in the Office Action, "to obtain a light emitting device with improved efficiency", is based upon impermissible hindsight, i.e. such a reason is based upon knowledge of the present invention.

Therefore neither *Chang et al. nor Shakuda et al.*, whether taken separately or in combination, teach or suggest "an upper electrode formed so as to be in contact with an exposed surface of the p-type layer of the semiconductor lamination portion exposed by removing a part of the light transmitting conductive layer, and to be in contact with the light transmitting conductive layer on a periphery of the part removed; and *an electric current blocking portion formed on the exposed surface of the semiconductor lamination portion*, the electric current blocking portion preventing electric current from flowing into a part of the semiconductor lamination portion under the upper electrode through the electric current blocking portion" as recited in claim 1.

As to claim 3, semiconductor layer **51** in FIG. 6 of *Chang et al.* does not contain oxygen, and a dielectric layer is simply buried therein, so that the semiconductor layer surface does not contain oxygen. Also, high resistance region **61** in FIG. 7 is formed by ion implantation; however, ions are implanted to a certain depth by ion implantation, and this is different from a layer in which the exposed surface of the semiconductor layer contains oxygen. Inherently, these current blocking regions are formed on the etch stop layer **24**, the transparent electrode **56** or the transparent conductive layer **63** is formed thereon, and the metal bonding layer **57B** or **65B** is formed thereon, so that it is completely different from a semiconductor layer surface that is in direct contact with the upper electrode and contains oxygen.

Claim 3 therefore patentably distinguishes over the combination of *Chang et al.* and *Shakuda et al.* for at least this additional reason.

Consequently, claims 1-4 are allowable over *Chang et al.* and *Shakuda et al.*

Newly added dependent claims 8-11 also contain allowable subject matter, as they add further features not disclosed in the art of record, and are allowable for at least the reasons that claim 1 is allowable.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should the remittance be accidentally missing or insufficient, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

December 5, 2008
Date

Alun L. Palmer – Registration No. 47,838
RABIN & BERDO, PC – Customer No. 23995
Facsimile: 202-408-0924
Telephone: 202-371-8976

ALP/pq